(54) **PULSE MODULATING METHOD, PULSE MODULATOR, AND PULSE DEMODULATOR**

(57) The present invention provides a pulse modulating method which ensures demodulation of bit data without being affected by a change in the pulse width and permits high-speed transmission, pulse modulating equipment for the pulse modulating method and pulse demodulating equipment. The pulse modulating equipment divides an input signal into n-bit words and converts it into a pulse unit signal which represents the state of the bit data for each word by time intervals i and j between odd-numbered transitions and between even-numbered transitions. The respective time intervals i and j are free from the influence of the transmission line used, for example, and remains unchanged in the pulse demodulating equipment, so that no demodulation error arises. Further, since the bit data is represented by the time intervals i and j between the odd-numbered transitions and between the even-numbered transitions, the coding efficiency increases, permitting high-speed transmission.

FIG. 1

2-bit data	transmission code		Pulse Unit Signal waveform	Pulse code
	i_i	j_i		
0 0	2T	2T		1 0 1 (0 1 0)
0 1	2T	3T		1 0 1 1 (0 1 0 0)
1 0	3T	2T		1 1 0 1 (0 0 1 0)
1 1	3T	3T		1 0 0 1 (0 1 1 0)

Description

TECHNICAL FIELD

The present invention relates to a method and equipment for modulating an input signal composed of bit data into a pulse signal, and pulse demodulating equipment.

BACKGROUND ART

There have heretofore been known, as pulse modulating methods of this kind, pulse amplitude modulation (PAM), pulse width modulation (PWM) and pulse phase modulation (PPM) methods which change the pulse amplitude, pulse width and pulse position of the pulse wave used as a carrier, respectively, in accordance with bit data.

In optical communication systems which use infrared rays and similar rays of light as carriers, the pulse amplitude modulation (PAM) which represents bit data by light intensity, in particular, has a problem with its reliability; therefore, the pulse width modulation (PWM) or pulse phase modulation (PPM) has been used in combination with other modulation methods.

Figs. 13(a) and (b) show signal waveforms by an ASK (Amplitude-Shift-Keying) system which is an example of such a combined use of different modulation methods. Digital data composed of a plurality of bit data is converted into a pulse signal (a) by an NRZ (Non-Return-to-Zero) modulation scheme which makes the digital data "L" (low) or "H" (high), depending on whether the bit data is "0" or "1" and the pulse signal (a) is used as a modulating wave for ASK modulation of a burst signal into a modulated wave (b).

In the case of demodulating the modulated wave (b), the envelope waveform of the burst signal is extracted from the input signal and is waveform shaped into the pulse signal (a), from which the plurality of bit data is demodulated by making marking and spacing portions of the pulse signal a "1" and a "0," respectively.

The ASK system represents 1-bit data by a pulse signal of a waveform of the same duration as that of the data, and hence it permits transmission of data in large quantities and is suitable for high-speed data transmission.

However, since the pulse width of the pulse signal (a) modulated by the NRZ modulation varies under the influence of frequency characteristics of the light emitting element, the light receiving element and the modem circuit and the transmission line used, the pulse width of the demodulated pulse signal does not always become the same as the pulse width of the modulated signal.

For example, the received waveform at the demodulating side may sometimes expand its pulse width because of a delay in the fall of the pulse waveform as indicated by a received waveform 1 in Fig. 14 or narrow its pulse width because of a delay in either of the rise and fall of the pulse waveform as indicated by a received waveform 2 in Fig. 14. That is, the pulse width C_0 of the transmitted waveform does not necessarily become the same as the pulse width C_1 or C_2 of the received waveforms 1 or 2.

In the demodulation of bit data from the pulse signal of such a varied pulse width, a shift in its pulse position causes a demodulation error.

On the other hand, there has also been known a PPM system which changes the time interval A_0 between leading edges of the modulated pulse signal according to the bit data, through utilization of the fact that the time width A_0 between leading edges of the pulse signal is equal to the time intervals A_1 and A_2 between the leading edges of the demodulated signals. As shown in Fig. 13(c), according to the PPM system, each bit data of the digital data is preceded by a pulse of a width T and the subsequent pulse quiescent period is represented by a time interval T or 3T, depending on whether the bit data is "0" or "1" and the thus converted pulse signal (c) is used as a modulating wave for the ASK modulation of the burst signal.

With the PPM system, demodulation errors decrease, but since each 1-bit data is represented by the pulse quiescent period, the frame transmission period for sending a plurality of bit data in its entirety is long, giving rise to the problem of low transmission rate.

As a solution to this problem, there has been developed such an SIR modulation system as shown in Fig. 13(d), which represents a plurality of bit data based on the position of respective leading edges of a pulse signal (d) so as to exclude the influence of pulse width variations and raise the transmission rate.

According to the SIR system, a plurality of bit data are divided into words each composed of 2-bit data and the leading edge or phase of a pulse of the width T is changed within a time interval 4T of the 2-bit data in accordance with its four kinds of states.

Even with this pulse modulation method, however, since the bit data is represented by the pulse leading edge alone, the level of redundancy is so high that there is a limit to an increase in the transmission rate.

The present invention is intended to solve the problems mentioned above and, based on the fact that while in Fig. 14 the pulse width C_0 in the received waveform differs from the width in the transmitted waveform, the time intervals A_0 and B_0 between the pulse leading edges and between the trailing edges remain substantially unchanged, the invention offers a pulse modulation method which represents bit data by the two kinds of time intervals A_0, B_0, increases the coding efficiency and permits demodulation free from the influence of the transmission system used.

That is, it is an object of the present invention to provide a pulse modulating method which ensures demodulation of bit data even if the pulse width varies, pulse modulating equipment therefor and pulse demodulating equipment.

Another object of the present invention is to provide a pulse modulating method which permits high-speed

transmission of bit data, pulse modulating equipment therefor and pulse demodulating equipment.

Another object of the present invention is to provide a pulse modulating method which is low in the level of redundancy and hence is high in coding efficiency and permits high-speed transmission.

Another object of the present invention is to provide a pulse modulating method which permits reduction of the frame transmission period for the transmission of bit data in its entirety.

Still another object of the present invention is to provide a pulse modulating method which allows ease in detecting an error during modulation and easy demodulation and, even if a transit signal is applied by noise or the like during demodulation of the current word, prevents it from affecting the demodulation of other words.

DISCLOSURE OF THE INVENTION

In a pulse modulating method according to an aspect of the present invention which converts an input signal composed of plural bit data into a modulated pulse signal: the input signal is divided into words each composed of n-bit data (n being a positive integer equal to or greater than 2); time intervals i_m and j_m (m being a positive integer starting with 1) are combined to form at least 2^n or more transmission codes; all states of the n-bit data are made to correspond to the transmission codes, respectively; in accordance with the transmission code corresponding to the state of the bit data for each word, the input signal is converted into pulse unit signals which have the time interval i_m between (2m-1)th and (2m+1)th transitions and the time interval j_m between (2m)th and (2m+2)th transitions; and the pulse unit signals thus converted in word units are concatenated into a modulated pulse signal.

With this method, the one of the time intervals i_m and j_m between transitions of the pulse unit signal converted for each word represents the time interval between respective leading edges of the pulse unit signal and the other the time interval between its respective trailing edges. The pulse width of the pulse unit signal varies under the influence of frequency characteristics of the light emitting element, the light receiving element and the modem circuit, but since each rise or fall of the pulse unit signal is affected under the same condition, the pulse signal that represents respective states of the bit data by the time intervals between the leading edges and between the trailing edges can be demodulated without being affected by the above-mentioned frequency characteristics.

Moreover, since the state of the n-bit data is represented by both of the time intervals between the leading edges and between the trailing edges of the pulse unit signal, redundancy is eliminated and the coding efficiency is increased, permitting high-speed transmission of bit data.

In a pulse modulating method according to another

aspect of the present invention, the first transition of each pulse unit signal is the last transition of the immediately preceding pulse unit signal.

With this method, the first transition of the pulse unit signal of each word may be a rise or fall of the pulse. That is, the current pulse unit signal can be concatenated with the immediately preceding pulse unit signal, using the last transition of the latter as the first transition of the former, whether it is a rise or fall of the pulse. Since the last transition of the immediately preceding pulse unit signal can be used to concatenate therewith the current pulse unit signal, the frame transmission period for transmitting the entire bit data can be shortened.

In a pulse modulating method according to another aspect of the present invention, the input signal is divided in units of words each composed of 2-bit data, time intervals i_1 and j_1 are selected from 2T and 3T, T being a unit time interval, the time intervals i_1 and j_1 are combined into four different transmission codes, and the input signal is converted into pulse unit signals, each having the time intervals i_1 and j_1 between first and third transitions and between second and fourth transitions, respectively.

With this method, the four states of the 2-bit data can be made to correspond to the four transmission codes which are combinations of the time intervals 2T and 3T. The time intervals i_1 and j_1 between the first and third transitions of the pulse unit signal and between its second and fourth transitions are either 2T or 3T, and letting the pulse width be represented by T, the duration of the pulse unit signal is 3T or 4T. Thus, the period for transmitting all of the bit data can be reduced.

In a pulse modulating method according to another aspect of the present invention, the input signal is divided in units of words each composed of 4-bit data, time intervals i_1 and j_1 are selected from 2T, 2.5T, 3T and 3.5T, T being a unit time interval, the time intervals i_1 and j_1 are combined into 16 different transmission codes, and the input signal is converted into pulse unit signals, each having the time intervals i_1 and j_1 between its first and third transitions and between its second and fourth transitions, respectively.

With this method, 16 kinds of states of the 4-bit data can be made to correspond to the 16 kinds of transmission codes which are combinations of 2T, 2.5T, 3T and 3.5T. The time intervals i_1 and j_1 between the first and third transitions of the pulse unit signal and between its second and fourth transitions are any one of 2T, 2.5T, 3T and 3.5T, and letting the pulse width be represented by T, the duration of each pulse unit signal is in the range of 3T to 4.5T. Thus, the period for transmitting all of the bit data in the can be reduced.

According to another aspect of the present invention, the unit time interval T is the data width of 1-bit data.

According to another aspect of the present invention, the time interval F between first and last transitions of each pulse unit signal is constant.

With this method, since the duration F of each pulse unit signal is constant, the period for transmitting all of the bit data is also constant, allowing ease in detecting a demodulation error. Further, since the modulated signal can be demodulated into bit data of each word at the time intervals F, the demodulation is easy and, even if a transit signal is applied by noise or the like, it does not affect the demodulation of other words.

In a pulse modulating method according to another aspect of the present invention, 2^n kinds of NRZ signals are assumed which were NRZ modulated by (n+2) pieces of bit data whose most and least significant bits are "1s" in common to them but whose intermediate bits differ from one another, and time intervals between (2m-1)th and (2m+1)th transitions and between its (2m)th and (2m+2)th transitions of each NRZ signal are combinations of the time intervals i_m and j_m and the time interval F is used as the duration of NRZ signal which were NRZ modulated by (n+2) pieces of bit data.

With this method, the 2^n kinds of NRZ signals are pulse signals that correspond to all different data of the intermediate n-bit data. The NRZ signals have the time interval between transitions at their opposite ends defined by the time interval of the (n+2) bit data but differ in the intermediate pulse waveform and in the combination of time intervals between their odd-numbered transitions and between their even-numbered transitions. Hence, by defining the combinations of these time intervals by the combinations of the time intervals i_m and j_m, it is possible to obtain 2^n kinds of transmission codes which provide pulse unit signals of the fixed duration F.

Pulse modulating equipment according to another aspect of the present invention comprises: a serial-parallel converter which divides a serial input signal composed of a plurality of bit data in steps of n bits (n being a positive integer equal to or greater than 2) and outputs the input signal as n-bit parallel data; an encoded table storage circuit which obtains at least 2^n kinds of different transmission codes by combining time intervals i_m and j_m (m being a positive integer beginning with 1) and wherein pulse codes which has time intervals between (2m-1)th and (2m+1)th transitions and between (2m)th and (2m+2)th transitions of pulse unit signals defined by i_m and j_m, respectively, in accordance with the transmission codes are stored in correspondence with respective states of n-bit parallel data; an encoder circuit which reads out the pulse code corresponding to the n-bit parallel data from the encoded table storage circuit and outputs it; a pulse signal generator which generates pulse unit signals from the pulse codes and outputs them serially; and a pulse output circuit which concatenates the pulse unit signals converted every n-bit parallel data into a pulse signal and outputs it.

With this construction, a plurality of bit data are divided by the serial-parallel converter into n-bit parallel data. The encoder circuit supplies the pulse signal generator with pulse codes corresponding to the states of n-bit parallel data. Based on the pulse codes, the pulse

signal generator serially outputs pulse unit signals which has the time intervals between odd-numbered transitions and between even-numbered transitions defined as i_m and j_m, respectively. The pulse output circuit outputs the pulse signal into which the pulse unit signals are concatenated.

Hence, the bit data of the n-bit parallel data is represented by the time intervals between trailing edges of the pulse unit signal and between its leading edges, and even if the pulse width changes under the influence of the state of transmission, it is possible to output a pulse signal free from a demodulation error.

Pulse demodulating equipment according to another aspect of the present invention comprises: a transition detecting circuit which divides an input pulse signal every fixed number K of transitions and, for each pulse unit signal defined by the K transitions, repeatedly detects the time intervals i_m and j_m between the (2m-1)th (m being a positive integer beginning with 1) and (2m+1)th transitions and between the (2m)th and (2m+2)th transitions; a decoded table storage circuit wherein at least 2^n (n being a positive integer equal to or greater than 2) different combinations of time intervals i_m and j_m (m being a positive integer in the range of 1 to k) are stored in correspondence with respective states of the n-bit data; a decoder circuit which reads out the n-bit data from the decoded table storage circuit corresponding to the combination of the time intervals i_m and j_m detected by the transition detecting circuit and outputs it as n-bit parallel data; and a parallel-serial converter which converts each n-bit parallel data demodulated for each pulse unit signal into a serial signal and outputs it as a signal composed of a plurality of bit data.

With this construction, the input pulse signal is divided every fixed number K of transitions. By setting the number K to be equal to the number of inversions of the pulse unit signal converted from the n-bit data, the input pulse signal is divided into pulse unit signals. The transition detecting circuit detects, for each pulse unit signal, the time intervals i_m and j_m between its odd-numbered transitions and between its even-numbered transitions.

The decoder circuit reads out the n-bit data from the decoded table storage circuit corresponding to the combination of the time intervals i_m and j_m and outputs it as n-bit parallel data. The n-bit parallel data are converted by the parallel-serial converter into a serial signal of n-bit data, which is concatenated with a serial signal of n-bit data similarly demodulated from the immediately preceding pulse unit signal, obtaining an output signal composed of plural bit data.

Hence, bit data can be demodulated from the pulse signal representing the plural bit data by the time intervals between the trailing edges and between leading edges, and even if the pulse width changes under the influence of the state of transmission, no demodulation error will arise.

Moreover, even if the pulse unit signals converted

from the n-bit data have different durations, it is possible to divide the input pulse signal into pulse unit signals by adjusting the number K of transitions and demodulate the pulse signal for each pulse unit signal.

Pulse demodulating equipment according to another aspect of the present invention comprises: a transition detecting circuit which divides an input pulse signal at fixed time intervals F and, for each pulse unit signal defined by the duration F, detects time intervals i_m and j_m between (2m-1)th (m being a positive integer beginning with 1) and (2m+1)th transitions and between (2m)th and (2m+2)th transitions; a decoded table storage circuit wherein at least 2^n (n being a positive integer equal to or greater than 2) different combinations of time intervals i_m and j_m (m being a positive integer in the range of 1 to k) are stored in correspondence with respective states of the n-bit data; a decoder circuit which reads out the n-bit data from the decoded table storage circuit corresponding to the combination of the time intervals i_m and j_m detected by the transition detecting circuit and outputs it as n-bit parallel data; and a parallel-serial converter which converts each n-bit parallel data demodulated for each pulse unit signal into a serial signal and outputs it as a signal composed of a plurality of bit data.

With this construction, the input pulse signal is divided at fixed time intervals F. By setting the duration F to be equal to the duration of each pulse unit signal converted from the n-bit data, the input pulse signal is divided into pulse unit signals. The transition detecting circuit detects, for each pulse unit signal, the time intervals i_m and j_m between its odd-numbered transitions and between its even-numbered transitions. The decoder circuit reads out the n-bit data from the decoded table storage circuit corresponding to the combination of the time intervals i_m and j_m and outputs it as n-bit parallel data. The n-bit parallel data are converted by the parallel-serial converter into a serial signal of n-bit data, which is concatenated with a serial signal of n-bit data similarly demodulated from the immediately preceding pulse unit signal, obtaining an output signal composed of plural bit data.

Hence, bit data can be demodulated from the pulse signal representing the plural bit data by the time intervals between the trailing edges and between leading edges, and even if the pulse width changes under the influence of the state of transmission, no demodulation error will arise.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is an explanatory diagram showing four kinds of states of 2-bit data and the relationships thereto of transmission codes and pulse codes in a 2-bit variable length system according to a first embodiment of the present invention; and Fig. 2 is an explanatory diagram showing the procedure for generating pulse unit signals in accordance weth following the transmission codes;

Fig. 3 is a block diagram illustrating the configuration of pulse modulating equipment 1 for use in the 2-bit variable length system according to the present invention; and Fig. 4 is a block diagram illustrating pulse demodulating equipment for demodulating plural bit data from a pulse signal converted by the 2-bit variable length system according to the present invention;

Fig. 5 is a waveform diagram showing, in comparison, a pulse signal converted by a conventional pulse modulating method and a pulse signal converted by the pulse modulating method according to the present invention, with the minimum width T of each pulse signal set at 1/2 the data width of the input signal; and Fig. 6 is a waveform diagram showing, in comparison, a pulse signal converted by a conventional pulse modulating method and a pulse signal converted by the pulse modulating method according to the present invention, with the minimum width T of each pulse signal set to be equal to the data width of the input signal;

Fig. 7 is a diagram for explaining processing in a decoder circuit 13;

Fig. 8 is an explanatory diagram showing 16 kinds of states of 4-bit data and the relationships thereto of transmission codes and pulse codes in a 4-bit variable length system according to a second embodiment of the present invention; and Fig. 9 is an explanatory diagram showing 16 kinds of states of 4-bit data and the relationships thereto of transmission codes and pulse codes in a 4-bit fixed length system according to a third embodiment of the present invention;

Fig. 10 is a block diagram illustrating the configuration of pulse modulating equipment 17 for use in the 4-bit fixed length system according to the present invention; and Fig. 11 is a block diagram illustrating the configuration of pulse demodulating equipment 18 for use in the 4-bit fixed length system according to the present invention;

Fig. 13 is a diagram for explaining processing in a decoder circuit 22;

Fig. 13 is a waveform diagram showing a conventional pulse modulating method; and Fig. 14 is a waveform diagram showing the relationships between transmitted and received waveforms.

BEST MODE FOR CARRYING OUT THE INVENTION

A description will be given, with reference to Figs. 1 through 6, of a pulse modulating method according to a first embodiment of the present invention.

Fig. 1 shows four kinds of states of two-bit data and

the relationships between the four kinds of states and transmission and pulse codes corresponding thereto.

In this embodiment, an input signal composed of plural bit data is divided into words of two-bit data and pulse modulation is carried out for each two-bit data to obtain a pulse unit signal.

As depicted in Fig. 1, each two-bit data assumes one of four different states and transmission codes (i_1, j_1) which are four kinds of combinations of time intervals 2T and 3T are each assigned to one of the four states.

The transmission code i_1 represents the time interval between first and third transitions and j_1 the time interval between second and fourth transitions. Reference character T denotes a unit time interval, which is equal to the minimum pulse width and the minimum pulse quiescent time of the pulse unit signal.

Accordingly, when the two-bit data of one word is, for example, "1,0," the time intervals between the first and third transitions r_1 and r_3 and between the second and fourth transitions r_2 and r_4 are 3T and 2T, respectively, and the minimum pulse width and the minimum pulse quiescent time are T as shown in Fig. 1; thus, the pulse code which forms the pulse unit signal is "1101."

Referring now to Fig. 2, the procedure for forming the pulse unit signal based on the transmission codes will be described.

In the first place, the time interval between the first and third transitions r_1 and r_3 is determined based on the transmission code i_1 (a).

Next, the transmission codes i_1 and j_1 are compared and when $j_1 \geq i_1$, a point in time which is the unit time T behind the first transition r_1 is set as the point of second transition r_2 (b1).

Then, a point in time which is behind the second transition r_2 by the time corresponding to the transmission code j1 is set as the point of fourth transition r_4; thus, a pulse unit signal is obtained which transits its level at these four points in time (c1).

On the other hand, when $j_1 < i_1$, a point in time which is the unit time T behind the third transition r_3 is set as the point of fourth transition r_4 (b2).

Following this, a point in time which is ahead of the fourth transition r_4 by the time corresponding to the transmission code j_1 is set as the point of second transition r_2; thus, a pulse unit signal is obtained which transits its level at these four points in time (c2).

In this way, the two-bit data forming each word is converted into one of four kinds of pulse unit signals each composed of three or four bits. (The pulse modulating method according to this embodiment will hereinafter be referred to as a two-bit variable length system.)

Incidentally, the pulse unit signals thus converted in word units are concatenated into a sequence of pulse signals. In this instance, the pulse unit signals are concatenated using the last transition (the fourth transition r4 in this embodiment) of the immediately preceding pulse unit signal as the first transition r1 of the immediately following pulse unit signal. Hence, the pulse unit signals of odd-numbered words rise at the points of first

transitions r1 as shown in Figs. 1 and 2, whereas the pulse unit signals of even-numbered words concatenated with them fall at the points of first transitions r1, and consequently, their pulse waveforms are opposite in level to those shown in Figs. 1 and 2 and their pulse codes are also opposite to those shown therein.

Figs. 5(d) and 6(b) show the waveforms of pulse signals converted using the two-bit variable length system according to the present invention, Fig. 5 showing the waveform with the unit time T (the minimum pulse width of the pulse signal) set at half the data width of the input signal and Fig. 6 the waveform with the unit time T set at a value equal to the data width of the input signal.

Assuming that the input signal is 16-bit data such as shown in Figs. 5 and 6, the pulse signal converted by the two bit variable length system is 30-bit pulse signal, and as is evident from Fig. 5, its transmission period is about twice longer than in the case of the NRZ modulation (a) but about half that in the case of the PPM modulation (b) and a little shorter than in the case of the SIR system.

Fig. 3 is a block diagram illustrating the configuration of pulse modulating equipment 1 according to the present invention, which will be described as being applied to the conversion of the input signal into a pulse signal by the above-described two-bit variable length system.

In Fig. 3, a serial input signal composed of plural bit data is input into a serial-parallel converter 3 via a buffer 2. The buffer 2 temporarily stores the serial input signal and outputs it as the serial-parallel conversion proceeds in the serial-parallel converter 3. The serial-parallel converter 3 converts the serial input signal from the buffer 3 into parallel data in word units of two-bit data for input into an encoder 4.

The encoder 4 is provided with an encoded table storage circuit 4a wherein the respective states of two-bit data and the pulse codes, such as shown in Fig. 1, are stored in correspondence with each other. As described previously, the pulse codes, based on the transmission codes i_1 and j_1 corresponding to the two-bit data, each form a pulse unit signal which has the time interval i_1 between odd-numbered transitions and the time interval j_1 between even-numbered transit positions.

The encoder 4 reads out the pulse codes corresponding to the two-bit parallel data inputted thereto from the encoded table storage, circuit 4a and provides them to a parallel-serial converter 5 that serves as a pulse signal generator.

For example, if the two-bit parallel data is "0,1," a pulse code of four bits "1011" is output.

In this instance, if the least significant bit LSB of the immediately preceding pulse code is "1," the above pulse code is inverted to "0100." The reason for this is that since the least significant bit LSB of the pulse code of the odd-numbered word is a "1" to form the last transition r4 of the pulse unit signal as a falling edge, the pulse code of the immediately subsequent even-num-

bered word is inverted and the falling edge of the preceding pulse unit signal is used as the first transition of the pulse unit signal immediately subsequent thereto.

Reference numeral 30 denotes a timing generator connected between the output of the encoder 4 and the input of the serial-parallel converter 3, for controlling the output from the serial-parallel converter 3 in accordance with the pulse code output state of the encoder 4. That is, the pulse codes that are output from the encoder 4 are codes of different lengths of three and four bits and when the four-bit pulse code is output, the output timing of the serial-parallel converter 3 is delayed by one bit.

Based on the pulse codes, the parallel-serial converter 5 generates pulse unit signals and serially applies them to a transmitter circuit 6. The transmitter circuit 6 is provided with a pulse output circuit, by which the pulse unit signals output in word units are concatenated into a serial converted pulse signal. The transmitter circuit 6 is further provided with an infrared-emitting circuit which emits infrared rays according to the pulse signal; the infrared rays containing the serial converted pulse signal are emitted to pulse demodulating equipment 7.

Fig. 4 is a block diagram of the pulse demodulating equipment 7 which receives the infrared rays containing the pulse signal and demodulates it into a plurality of bit data.

When received by a receiver circuit 8, the infrared rays containing the pulse signal are subjected to photoelectric conversion and then waveform shaped into a pulse signal. The output of the receiver circuit 8 is connected to a rise detector 9 and a fall detector 10 for detecting the rise and fall of the pulse signal which is output from the receiver circuit 8.

Upon detection of the rise of the pulse signal, the rise detector 9 applies the rise detection signal to a first counter 11 connected to the output thereof.

The first counter 11 always counts clock signals from a clock generator 12 and, when supplied with the rise detection signal, provides the current count value as a first count value UC to a decoder 13, while at the same time it resets its count value to zero and resumes counting the clock signals. That is, the first count value UC from the first counter 11 represents the time interval between two successive rising or leading edges of the pulse signal.

On the other hand, upon detection of the fall of the pulse signal, the fall detector 9 applies the fall detection signal to a second counter 14 connected to the output thereof.

The second counter 14 always counts the clock signals from the clock generator 12 as is the case with the first counter 11 and, when supplied with the fall detection signal, provides the current count value as a second count value DC to the decoder 13, while at the same time it resets its count value to zero and resumes counting the clock signals. The second count value DC from the second counter 14 represents the time interval between two successive trailing or falling edges of the pulse signal.

The decoder 13 is provided with a decoded table storage circuit 13a wherein combinations of transmission codes, each composed of the time intervals i_1 and j_1 between the first and third transitions r_1 and r_3 and between the second and fourth transitions r_2 and r_4, are stored in correspondence with the respective states of the two-bit data. The correspondence between the combinations of the transmission codes i_1 and j_1 and the two-bit data in the decoded table storage circuit 13a is the same as the correspondence between the transmission codes i_1 and j_1 and the two-bit data in the encoded table storage circuit 4a of the pulse modulating equipment 1 (see Fig. 1).

The decoder 13 detects the combination of the transmission codes i_1 and j_1 from the first and second count values UC and DC and reads out the two-bit data corresponding to the detected combination of the transmission codes from the decoded table storage circuit 13a.

Turning to Fig 7, the processing in the decoder 13 will be described below.

Provided that the pulse signal fed thereto from the receiver circuit 8 is a pulse signal of such a waveform as shown in Fig. 7, the decoder 13 detects the combination of the transmission codes i_1 and j_1 for each pulse unit signal converted from the two-bit data. In the case of pulse modulation by the two-bit variable length system, the pulse unit signal have four transitions and the first and fourth transitions are common to the pulse unit signals immediately preceding and succeeding the current one. Accordingly, the pulse signal can be split into pulse unit signals every third transitions.

As depicted in Fig. 7, upon each detection of the rise and fall of the pulse signal, the first and second count values UC and DC are alternately input into the decoder 13. Hence, whenever the first and second count values UC and DC are input into the decoder a total of three times, this point in time is regarded as the time when the pulse unit signals are concatenated and the first and second count values UC and DC input in this period between concatenated points are used to obtain transmission codes i_1 and j_1 of the pulse unit signal of this period.

As will be seen from Fig. 7, the count value input second in the above period represents the time interval between the first and third transitions of the pulse unit signal, that is, the transmission code i_1, and the count value input third in the above period represents the time interval between the second and fourth transitions of the pulse unit signal, that is, the transmission code j_1. In this way, the transmission codes i_1 and j_1 are derived from these count values.

In the case of a first pulse unit signal, the transmission codes i1 and j1 can be obtained from first and second count values UC1 and DC2, respectively. Assuming that the period of the clock signal from the clock generator 12 is 1/16 the unit time T of the pulse signal, the count value for the unit time T is 16, so that if the first

count value UC1 is within 48 ± 3, the transmission code i1 is 3T. Similarly, if the second count value DC2 is within 32 ± 3, the transmission code j1 is 2T.

Since the two-bit data corresponding to the combination (3T,2T) of the transmission codes i_1 and j_1 is "1,0," (as shwon in fig. 1) the two-bit data is fed as two-bit parallel data to a parallel-serial converter 15.

Likewise, the transmission codes i_1 and j_1 of the second pulse unit signal are derived from the second and first count values DC3 and UC3, respectively. Since the second and first count values DC3 and UC3 are both within 48 ± 3, the transmission codes i_1 and j_1 are (3T,3T), then the corresponding two-bit data "1,1" is readout, and two-bit parallel data "1,1" is fed to the parallel-serial converter 15.

The parallel-serial converter 15 converts the parallel data, output in units of two bits from the decoder 13, into serial signals and provides them to a buffer 16, which concatenates the serial signals and outputs them as a demodulated signal composed of a plurality of bits.

As described above, the pulse demodulating equipment 7 detects the time intervals between the leading or rising edges of the pulse signal and between its trailing or falling edges and demodulates the pulse signal into bit data. Hence, even if the pulse width changes under the influence of the transmission line or the frequency characteristics in the modem, the time intervals will not change and the demodulation can be achieved with accuracy.

Fig. 8 is a table explanatory of a pulse modulating method according to another embodiment of the present invention, showing 16 kinds of states of four-bit data and the relationships between them and the transmission codes i_1,j_1 and pulse codes corresponding thereto.

In this embodiment, an input signal composed of plural bit data is divided into words of four-bit data, which are each converted into a pulse unit signal of three through five bits according to the state of the four-bit data. (The pulse modulating method according to this embodiment will hereinafter be called a four-bit variable length system.)

As shown in Fig. 8, the number of data states of the 4-bit data is 16, 16 combinations of 2T, 2.5T, 3T and 3.5T corresponding to the respective data states are assigned to the transmission codes i_1 and j_1. When the unit time T is used as the minimum pulse width of the pulse unit signal and the minimum pulse quiescent time as mentioned above, the transmission codes i_1 and j_1 need not always be integral multiples of the unit time T.

For example, in case a 4-bit data divided into word is "1,0,0,1", the corresponding transmission codes i_1 and j_1 are 2.5T and 3T. The pulse unit signal that is generated based on such transmission codes has the time interval 2.5T between its first and third transitions r_1 and r_3 and the time interval 2T between its second and fourth transitions r2 and r_4, and the pulse code for generating the pulse unit signal is "11000111." No description will be given of the method for generating the pulse

unit signals based on the transmission codes since it is the same as that described previously with reference to Fig. 2. Incidentally, since the pulse unit signal is not a rectangular wave composed of integral bits, 1-bit pulse unit signal is represented by a 2-bit pulse code for the sake of convenience.

Also in this instance, the pulse unit signals are concatenated using the fourth transition r4 of the immediately preceding one of them as the first transition of the immediately succeeding pulse unit signal as is the case with the afore-mentioned 2-bit modulating system. Accordingly, the first inversion r1 of the pulse unit signal of an even-numbered word is the fall of the pulse, so that the pulse waveform is opposite in level to that shown in fig. 8 and the pulse code is also opposite.

Since the pulse unit signals are concatenated using the last inversion of the immediately preceding signal as the first inversion of the succeeding signal as mentioned above, the frame transmission period for transmitting the whole bit data can be reduced.

Figs. 5(e) and 6(c) show waveforms of the pulse signals converted by the 4-bit variable length system.

As will be seen from Figs. 5(e) and 6(c), the frame transmission period for transmitting the whole bit data is half that in the case of the 2-bit variable length system, substantially equal to that in the case of the NRZ modulating system and extremely shorter than in the cases of the PPM and SIR systems. By dividing the input signal into data of a larger number of bits in the pulse modulation, the entire transmission period can be further reduced.

The pulse modulating equipment 1 of Fig. 3 can be used in the 4-bit variable length system, by using an arrangement in which the serial-parallel converter 3 divides the input signal into words of 4-bit data and outputs 4-bit parallel data and the relationships between the bit data and the pulse codes shown in Fig. 8 are stored in the encoded table storage circuit 4a.

Further, the pulse demodulating equipment 7 of Fig. 4 can be used by storing in its decoded table storage circuit 13a the relationships between the bit data and the pulse codes shown in Fig. 8.

Fig. 9 is a table explanatory of a pulse modulating method according to further another embodiment of the present invention, showing 16 kinds of states of 4-bit data and the relationships thereto of transmission codes i_1, i_2, j_1, j_2 and pulse codes.

In this third embodiment, the input signal composed of plural bit data is divided into words of 4-bit data, each of which is converted into a 6-bit pulse unit signal of fixed length based on the state of the divided 4-bit data. (The pulse modulating method according to this embodiment will hereinafter be referred to as a 4-bit fixed length system.)

The transmission code i2 represents the time interval between third and fifth transition of the pulse unit signal and the transmission code j2 the time interval between its fourth and sixth transitions. As shown, the 16 kinds of pulse unit signals are all 6 bits long, and as

8

compared with the above-described variable length system, the number of transitions is six in the case of representing the 4-bit data including the transmission codes i2 and j2.

To obtain 16 variant kinds of transmission codes, in accordance with which pulse unit signals of fixed 6-bit length, NRZ signals are assumed which were NRZ-modulated by 6-bit data. The transmission codes are gained from the time intervals between leading edges and between trailing edges of the NRZ signals.

That is, 16 kinds of NRZ signals are assumed which were NRZ-modulated by 16 variant kinds of 6-bit data whose most and least significant bits MSB and LSB are "1s" and whose intermediate bits are variant 4-bit data. Since the NRZ signals have their most and least significant bits formed by NRZ modulated versions of bit data "1," the pulse unit signal have rising and trailing edges at their first and sixth bits but each has one of 16 variant kinds of different intermediate waveforms.

Hence, by deriving the transmission codes i_1, i_2, j_1, j_2 from the time intervals between odd-numbered transitions and between even-numbered transitions, 16 kinds of combinations are obtained and the pulse units signals based on the transmission codes have a fixed 6-bit length.

Also in this 4-bit fixed length system, the pulse unit signal converted from an even-numbered word has its waveform inverted and is concatenated with the intermediately preceding and succeeding pulse unit signals, using the transitions at the concatenations in common to them.

Figs. 5(f) and 6(d) show waveforms of pulse signals converted by the 4-bit fixed length system.

As is evident from Fig. 6, the 4-bit fixed length system permits high-speed transmission as compared with the PPM and SIR systems, and since the pulse unit signals are fixed at 6 bits, demodulation is easier than in the cases of the 2-bit and 4-bit variable length systems of the present invention. Further, even if an error arises in one word during its demodulation, it does not affect the pulse unit signals of other words, and hence it does not constitute an error over the entire demodulation.

Figs. 10 and 11 illustrate in block form pulse modulating equipment 17 and pulse demodulating equipment 18 that are used in the 4-bit fixed length system.

The pulse modulating equipment and the pulse demodulating equipment are substantially identical in construction with those 1 and 7 described previously in respect of Figs. 3 and 4; the same parts are identified by the same reference numerals and no description will be repeated.

A serial-parallel converter 19 of the pulse modulating equipment 17 divides the serial input signal from the buffer 4 into words of 4-bit data and outputs 4-bit parallel data to an encoder circuit 20.

The encoder circuit 20 reads out the pulse codes corresponding to the 4-bit parallel data from an encoded table storage circuit 20a having stored therein 4-bit data and pulse codes in correspondence with each other as

shown in Fig. 9, the pulse code thus read out being fed to the parallel-serial converter 5.

This pulse code is to form the pulse unit signal of the waveform shown in Fig. 9 based on the transmission codes i_1, i_2, j_1, j_2 corresponding to the state of the 4-bit data, and since the pulse unit signals have the 6-bit fixed length, the pulse codes that are output are all 6 bits long. Consequently, the timing generator 30 in the pulse modulating equipment 1 of the variable length system is unnecessary.

The pulse demodulating equipment 18 is provided with a third counter 21 which is supplied with the rise detection signal and the fall detection signal from the rise detector 9 and the fall detector 10. In order that the decoder circuit 22 divides the input pulse signal at regular time intervals F (the time intervals corresponding 6-bit data in the case of the 4-bit fixed length system) for the demodulation of each pulse unit signal, the third counter 21 begins to count clock signals at the start of the pulse unit signal and, upon each reception of the rise or fall detection signal, outputs the count value at that time as a third count value BC to a decoder circuit 22, thereby notifying the termination of the pulse unit signal.

That is, the decoder circuit 22 applies a reset signal to the third counter 21 at the start of the pulse unit signal (that is also the termination of the immediately preceding pulse unit signal) to cause the third counter to start counting the clock signals and, upon each input thereto of the third count value BC for each transition of the pulse signal, compared the third count value BC with the fixed time interval F (corresponding to 6 bits) and, when the third count value BC indicates nearly equal to the time interval of 6 bits, regards the transition at that time as the end of the pulse unit signal. Since the position of termination of the pulse unit signal is also used as the position of start of the immediately succeeding pulse unit signal, the decoder circuit applied the reset signal again to the third counter 21 to cause it to begin counting the clock signals.

The decoder circuit 22 is provided with a decoded table storage circuit 22a wherein there are stored the transmission codes i_1, i_2, j_1, j_2 and respective states of the 4-bit data in correspondence with each other as shown in Fig. 9. The transmission codes are detected from the pulse unit signal divided into each word by the above-described method and the 4-bit data corresponding to the transmission codes is read out from the decoded table storage circuit 22a. Then the 4-bit data is fed as parallel data to the parallel-serial converter 15.

Turning to Fig. 12, the above processing in the decoder circuit 22 will be described below.

Assuming that the pulse signal from the receiver circuit 8 has such a waveform as shown in Fig. 12, the decoder circuit 22 makes a comparison between the third count value BC which is output from the third counter 21 upon each transition of the pulse signal and the 6-bit duration. Provided that the period of the clock signal from the clock generator 12 is 1/16 the unit time or dura-

tion T of the pulse signal, the pulse unit signal whose 1-bit duration is equal to the unit time T indicates that the count value is $6 \times 16=96$ and has reached the end of the pulse unit signal. On the other hand, the third count value BC represents the time interval between the start of the pulse unit signal and its transition at the time when the third count value BC is output, and at the end of the pulse unit signal, the pulse unit signal transits its level, so that when the third count value BC is within 96 ± 3, the transition at that time can be regarded as the end of the pulse unit signal.

For example, during the input of the first pulse unit signal, one of third count values BC11, BC12 and BC13 are input upon each transition of the pulse signal; since the third count value BC13 is within 96 ± 3, the transition r4 is regarded as the end of the first pulse unit signal. Similarly, during the input of the third pulse unit signal, third count values BC31, ..., BC34, BC35 are input; since the third count value BC35 is within 96 ± 3, the transition r6 is regarded as the end of the third pulse unit signal.

As is evident from Fig. 12, the count value input second from the first counter 11 or second counter 14 during the period of each pulse unit signal represents the time interval between first and third transitions, that is, the transmission code i_1; similarly, the count value input third represents the transmission code j_1, the count value input fourth the transmission code i_2 and the count value input fifth the transmission code j_2.

Thus, the transmission codes i_1, i_2, j_1, j_2 contained in each pulse unit signal are detected from these count values UC and DC.

For example, in the second pulse unit signal, the transmission code i_1 is represented by the second count value DC3 and the transmission code j_1 by the first count value UC3, and since the second and first count values DC3 and UC3 are within 64 ± 3 and within 80 ± 3, respectively, the transmission codes i_1 and j_1 of the second pulse unit signal are (4T,5T). Likewise, the transmission codes i_1, j_1, i_2, j_2 of the third pulse unit signal are (3T,3T,2T,2T) since the transmission code i_1 is represented by the first count value UC4, the transmission code j_1 by the second count value DC5, the transmission code i_2 by the first count value UC5 and the transmission code j_2 by the second count value DC6.

The 4-bit data whose transmission codes i_1 and j_1 correspond to the combination (4t,5T) is "0,0,0,1" as shown in Fig. 9 and this 4-bit data is read out of the decoded table storage circuit 22a and fed as 4-bit parallel data to the parallel-serial converter 15. The 4-bit data whose transmission codes i_1, j_1, i_2, j_2 correspond to the combination (3T,3T,2T,2T) is "0,0,1,0" as shown in Fig. 9 and this 4-bit data is read out of the decoded table storage circuit 22a and it is similarly fed as 4-bit parallel data to the parallel serial converter 15.

While in the embodiments of the present invention described above the last transition of each pulse unit signal is used as the first transition of the immediately succeeding pulse unit signal to concatenate the pulse

unit signal, their transitions need not always be used in common. In such a case, an odd-numbered transition can always be defined as the rise of the pulse signal and an even numbered transition as the fall of the pulse signal, so that the transmission codes i and j can be represented by combinations of the time intervals between leading edges and between railing edges of the pulse unit signal.

Furthermore, although in the embodiments of the invention the unit time T is used as the minimum pulse width of the pulse unit signal and as the minimum pulse quiescent time, the invention is not limited specifically thereto. By changing the unit time T, the frame transmission time for the converted pulse signal can be changed as desired.

The correspondence between respective states of bit data of each word and the transmission codes are not limited specifically to those shown in the drawings but other correspondence can be used as long as they have a one-to-one correspondence. In the third embodiment, in particular, the intermediate 4-bit data of the 6-bit data assumed to obtain combinations of transmission codes are made to correspond to the 4-bit data divided for each word so that they match each other, but the both bit data need not always to match each other.

INDUSTRIAL APPLICABILITY

As described above, the pulse modulating method, pulse modulating equipment and pulse demodulating equipment according to the present invention are suitable for use in optical communication system that employ infrared rays or similar rays of light as carriers.

Claims

1. A pulse modulating method which converts an input signal composed of plural bit data into a modulated pulse signal, characterized in:

   that the input signal is divided into words each composed of n-bit data (n being a positive integer equal to or greater than 2);

   that time intervals i_m and j_m (m being a positive integer starting with 1) are combined to form at least 2^n or more different transmission codes;

   that all states of the n-bit data are made to correspond to the transmission codes, respectively;

   that, in accordance with the transmission code corresponding to the state of the bit data for each word, the input signal is converted into pulse unit signals which have the time interval i_m between (2m-1)th and (2m+1)th transitions and the time interval j_m between (2m)th and (2m+2)th transitions; and

that the pulse unit signals thus converted in word units are concatenated into a modulated pulse signal.

2. A pulse modulating method as claimed in claim 1, characterized in that a first transition of each pulse unit signal is the last transition of the immediately preceding pulse unit signal.

3. A pulse modulating method as claimed in claim 1 or 2, characterized in:

that the input signal is divided in units of words each composed of 2-bit data;
that time intervals i_1 and j_1 are selected from 2T and 3T, T being a unit time interval;
that the time intervals i_1 and j_1 are combined into four different kinds of transmission codes; and
That the input signal is converted into pulse unit signals, each having the time intervals i_1 and j_1 between first and third transitions and between second and fourth transitions, respectively.

4. A pulse modulating method as claimed in claim 3, characterized in that the unit time interval T is the data width of 1-bit data.

5. A pulse modulating method as claimed in claim 1 or 2, characterized in:

that the input signal is divided in units of words each composed of 4-bit data;
that time intervals i_1 and j_1 are selected from 2T, 2.5T, 3T and 3.5T, T being a unit time interval;
that the time intervals i_1 and j_1 are combined into 16 different kinds of transmission codes; and
that the input signal is converted into pulse unit signals, each having the time intervals i_1 and j_1 between its first and third transitions and between its second and fourth transitions, respectively.

6. A pulse modulating method as claimed in claim 5, characterized in that the unit time interval T is the data width of 1-bit data.

7. A pulse modulating method as claimed in claim 1 or 2, characterized in that the time intervals F between the first and last transitions of the pulse unit signals are constant.

8. A pulse modulating method as claimed in claim 7, characterized in:

that 2^n kinds of NRZ signals are assumed

which were NRZ modulated by (n+2) pieces of bit data whose most and least significant bits are "1s" in common to them but whose intermediate bit data differ from one another;
that time intervals between (2m-1)th and (2m+1)th transitions and between its (2m)th and (2m+2)th transitions of each NRZ signal are combinations of the time intervals i_m and j_m; and
that the time interval F is used as the duration of NRZ signals which were NRZ modulated by (n-2) pieces of bit data.

9. Pulse modulating equipment characterized by:

a serial-parallel converter (3) (19) which divides a serial input signal composed of a plurality of bit data in steps of n bits (n being a positive integer equal to or greater than 2) and outputs the input signal as n-bit parallel data;

an encoded table storage circuit (4a) (20a) which obtains at least 2^n kinds of different transmission codes by combining time intervals i_m and j_m (m being a positive integer beginning with 1) and wherein pulse codes which has time intervals between (2m-1)th and (2m+1)th transitions and between 2m-th and (2m+2)th transitions of pulse unit signals defined by i_m and j_m, respectively, in accordance with the transmission codes are stored in correspondence with respective states of n-bit parallel data;

an encoder circuit (4) (20) which reads out the pulse code corresponding to the n-bit parallel data from the encoded table storage circuit and outputs it;

a pulse signal generator (5) which generates pulse unit signals from the pulse codes and outputs them serially; and

a pulse output circuit (6) which concatenates the pulse unit signals converted every n-bit parallel data into a pulse signal and outputs it.

10. Pulse demodulating equipment characterized by:

a transition detecting circuit (13) which divides an input pulse signal every fixed number K of transitions and, for each pulse unit signal defined by the K transitions, repeatedly detects time intervals i_m and j_m between (2m-1)th (m being a positive integer beginning with 1) and (2m+1)th transitions and between (2m)th and (2m+2)th transitions;
a decoded table storage circuit (13a) wherein at least 2^n (n being a positive integer equal to

or greater than 2) different combinations of
time intervals i_m and j_m (m being a positive inte-
ger in the range of 1 to k) are stored in corre-
spondence with respective states of the n-bit
data;

5

a decoder circuit (13) which reads out the n-bit
data from the decoded table storage circuit cor-
responding to the combination of the time inter-
vals i_m and j_m detected by the transition
detecting circuit and outputs it as n-bit parallel
data; and

10

a parallel-serial converter (15) which converts
each n-bit parallel data demodulated for each
pulse unit signal into a serial signal and outputs
it as a signal composed of a plurality of bit data.

15

11. Pulse demodulating equipment characterized by:

a transition detecting circuit (13) which divides
an input pulse signal at fixed time intervals F

20

and, for each pulse unit signal defined by the
duration F, detects time intervals i_m and j_m
between (2m-1)th (m being a positive integer
beginning with 1) and (2m+1)th transitions and
between (2m)th and (2m+2)th transitions;

25

a decoded table storage circuit (22a) wherein
at least 2^n (n being a positive integer equal to
or greater than 2) different combinations of
time intervals i_m and j_m are stored in corre-

30

spondence with respective states of the n-bit
data;

a decoder circuit (22) which reads out the n-bit
data from the decoded table storage circuit cor-

35

responding to the combination of the time inter-
vals i_m and j_m detected by the transition
detecting circuit and outputs it as n-bit parallel
data; and

40

a parallel-serial converter (15) which converts
each n-bit parallel data demodulated for each
pulse unit signal into a serial signal and outputs
it as a signal composed of a plurality of bit data.

45

50

55

12

FIG. 1

2-bit data	transmission code		Pulse unit Signal waveform	Pulse code
	i_1	j_1		
0 0	2 T	2 T		1 0 1 (0 1 0)
0 1	2 T	3 T		1 0 1 1 (0 1 0 0)
1 0	3 T	2 T		1 1 0 1 (0 0 1 0)
1 1	3 T	3 T		1 0 0 1 (0 1 1 0)

FIG. 2

a		
b 1		b 2
c 1		c 2

FIG. 3

input signal o— [buffer] — [Serial-Prallel converter]

2 — buffer
3 — Serial-Prallel converter
30 — タイミングジェネレータ — timing generator

符 号 化 回 路
(符号化テーブル
記憶回路 4 a) — (可変長コード)

1 —→

Parallel-serial Converter

4 — encorder (encorded table storag. circuit 4a)

並列－直列変換 —— 5

transmitter circuit

送 信 回 路 —— 6

FIG. 4

receiver circuit
受 信 回 路 —— 8

7 —→

9 rise detecta
立 上 り 検 出

10 fall detector
立 下 り 検 出

12 クロックジェネレータ
clock generator

11 first counter
第 1 カウンタ

第 2 カウンタ — Second counter

14

復 号 化 回 路
(復号化テーブル
記憶回路 13 a) —— 13

decorder (decoded table storage circuit)

16
data
データ o— [buffer] — 並列－直列変換 —— 15

Parallel- serial converter

FIG. 5

bit data

ビットデータ	1	0	1	1	0	0	1	0	0	1	0	0	1	1
(a) NRZ変調														
(b) PPM変調														
(c) SIR方式														
(d) 本発明 2ビット 可変長方式														
(e) 本発明 4ビット 可変長方式														
(f) 本発明 4ビット 固定長方式														

NRZ modulation

PPM modulation

SIR system

two-bit variable length system

4-bit variable length system

4-bit fixed length system

15

FIG. 6

bit data

ビットデータ

(a)	NRZ変調
(b)	本発明 2ビット 可変長方式
(c)	本発明 4ビット 可変長方式
(d)	本発明 4ビット 固定長方式

NRZ modulation

two-bit variable length system

4-bit variable length system

4-bit fixed length system

ビットデータ

bit data

FIG. 7

FIG. 8

4-bit data · transmission code · Pulse unit waveform · Pulse code

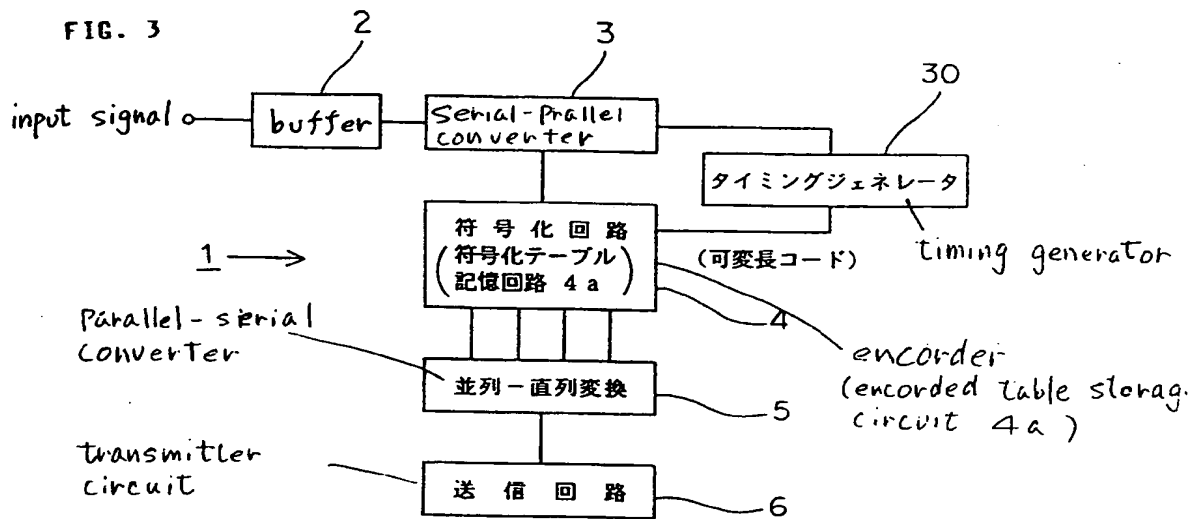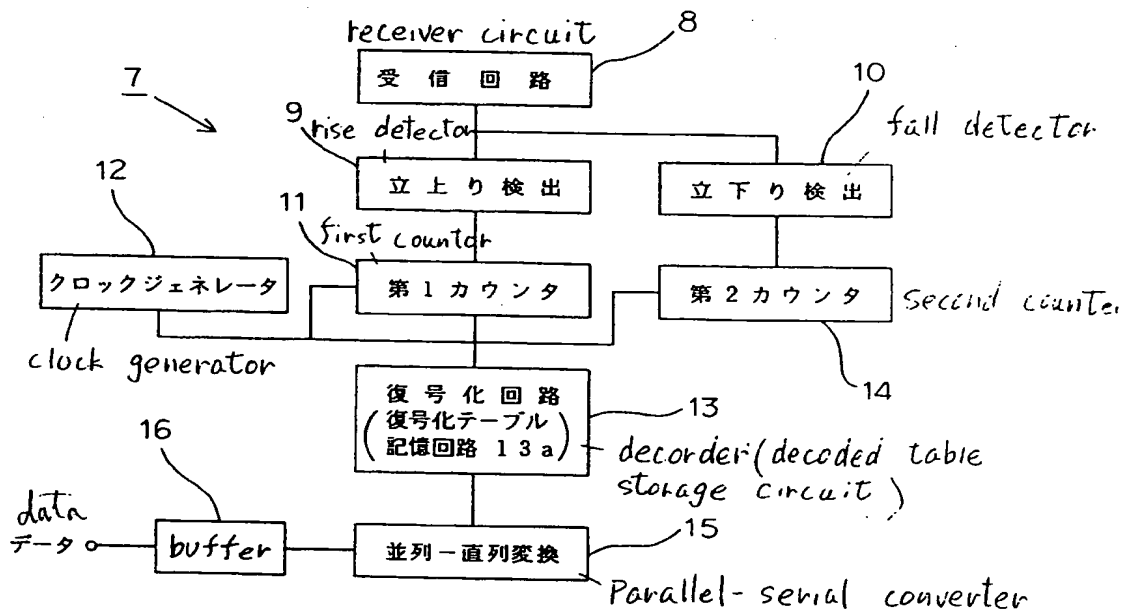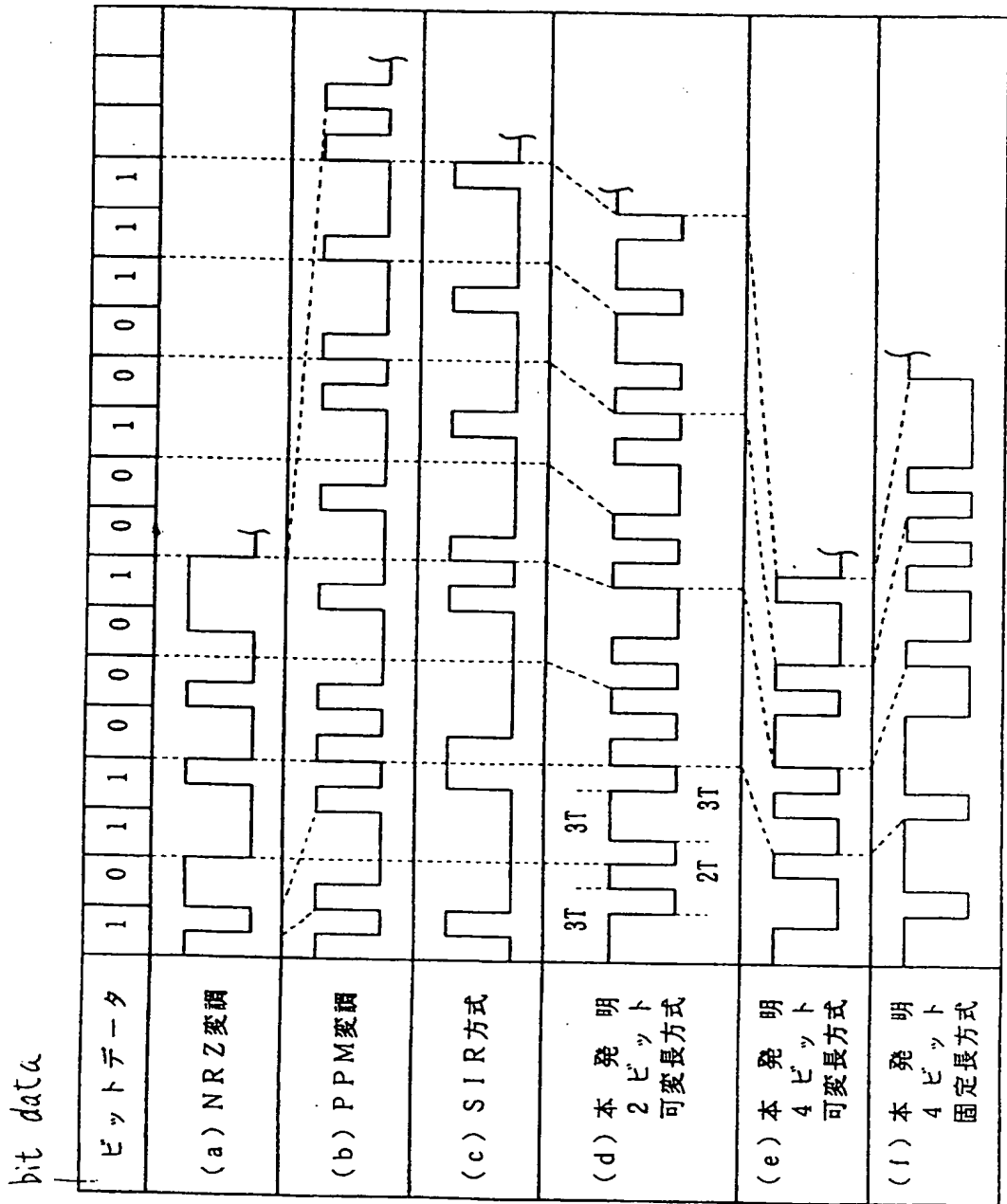| 4ビットデータ	伝送符号		パルスユニット波形	パルス符号
	i_1	j_1		
0 0 0 0	2 T	2 T		1 1 0 0 1 1
0 0 0 1	2.5 T	2 T		1 1 1 0 0 1 1
0 0 1 0	3 T	2 T		1 1 1 1 0 0 1 1
0 0 1 1	3.5 T	2 T		1 1 1 1 1 0 0 1 1
0 1 0 0	2 T	2.5 T		1 1 0 0 1 1 1
0 1 0 1	2.5 T	2.5 T		1 1 0 0 0 1 1
0 1 1 0	3 T	2.5 T		1 1 1 1 0 0 1 1
0 1 1 1	3.5 T	2.5 T		1 1 1 1 1 0 0 1 1
1 0 0 0	2 T	3 T		1 1 0 0 1 1 1 1
1 0 0 1	2.5 T	3 T		1 1 0 0 0 1 1 1
1 0 1 0	3 T	3 T		1 1 0 0 0 0 1 1
1 0 1 1	3.5 T	3 T		1 1 1 0 0 0 0 1 1
1 1 0 0	2 T	3.5 T		1 1 0 0 1 1 1 1 1
1 1 0 1	2.5 T	3.5 T		1 1 0 0 0 1 1 1 1
1 1 1 0	3 T	3.5 T		1 1 0 0 0 0 1 1 1
1 1 1 1	3.5 T	3.5 T		1 1 0 0 0 0 0 1 1

FIG. 9

4-bit data   transmission code   Pulse unit waveform   Pulse code

4ビットデータ	伝送符号				パルスユニット波形	パルス符号
	i_1	j_1	i_2	j_2		
0 0 0 0	5 T	5 T	—	—		1 0 0 0 0 1
0 0 0 1	4 T	5 T	—	—		1 0 0 0 1 1
0 0 1 0	3 T	3 T	2 T	2 T		1 0 0 1 0 1
0 0 1 1	3 T	5 T	—	—		1 0 0 1 1 1
0 1 0 0	2 T	2 T	3 T	3 T		1 0 1 0 0 1
0 1 0 1	2 T	2 T	2 T	3 T		1 0 1 0 1 1
0 1 1 0	2 T	3 T	3 T	2 T		1 0 1 1 0 1
0 1 1 1	2 T	5 T	—	—		1 0 1 1 1 1
1 0 0 0	5 T	4 T	—	—		1 1 0 0 0 1
1 0 0 1	4 T	4 T	—	—		1 1 0 0 1 1
1 0 1 0	3 T	2 T	2 T	2 T		1 1 0 1 0 1
1 0 1 1	3 T	4 T	—	—		1 1 0 1 1 1
1 1 0 0	5 T	3 T	—	—		1 1 1 0 0 1
1 1 0 1	4 T	3 T	—	—		1 1 1 0 1 1
1 1 1 0	5 T	2 T	—	—		1 1 1 1 0 1
1 1 1 1	—	—	—	—		1 1 1 1 1 1

FIG. 10

buffer   serial-parallel converter

o—| バッファ |—| 直 並 列 変 換 | 19   / 17

2

符 号 化 回 路
（符号化テーブル）
（記憶回路 ２０ａ）   20 encorder circuit
(encorded table storage circuit)

並列－直列変換   5   Parallel-serial converter

送 信 回 路   6   transmitter circuit

FIG. 11

receiver circuit

8   受 信 回 路

rise detector   fall detector

clock generator 9   立上り検出   立下り検出   10   second counter 21

12   11 first counter   14

クロックジェネレータ   第１カウンタ   第２カウンタ   第３カウンタ

third counter

22   復 号 化 回 路
（復号化テーブル）
（記憶回路 ２２ａ）   (decoded table storage circuit)

16 decoder circuit

o—| バッファ |—| 並列－直列変換 | 15

buffer   Parallel-serial converter

FIG. 12

	$UC_1(3T)$	$DC_1(4T)$	$UC_2(3T)$	$UC_4(3T)$	$DC_7(2T)$
i_1	$UC_1(3T)$	$DC_3(4T)$		$UC_4(3T)$	$DC_7(2T)$
J_1	$DC_2(4T)$	$UC_3(5T)$		$DC_5(3T)$	$UC_7(5T)$
i_2	—	—		$DC_6(3T)$	—
J_2	—	—		$DC_6(3T)$	—
4ビットデータ	1011	0001		0010	0111

4-bit data

FIG. 13

FIG. 14

bit data

ビットデータ		1	1	0	1	0	1	0	1	
transmitted waveform 送信波形										
received waveform 1 受信波形1										
received waveform 2 受信波形2										

A0　C0　B0

A1　C1　B1

A2　C2　B2

23

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP96/03040

A. CLASSIFICATION OF SUBJECT MATTER
Int. Cl^6 H03M7/14, H03M5/12, H04L25/49
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED
Minimum documentation searched (classification system followed by classification symbols)
Int. Cl^6 H03M7/14, H03M5/12, H04L25/49

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched	
Jitsuyo Shinan Koho	1926 - 1996
Kokai Jitsuyo Shinan Koho	1971 - 1996

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	JP, 5-227035, A (Nissan Motor Co., Ltd.), September 3, 1993 (03. 09. 93) & US, 5315299, A & DE, 4304305, C2 (Refer to column 1, line 38 to column 2, line 26; column 4, lines 5 to 39; column 6, line 49 to column 8, line 35; Figs. 1, 2, 5)	1 - 11
Y	JP, 52-23706, B (International Business Machines Corp.), June 25, 1977 (25. 06. 77) & US, 3701111, A & DE, 2205422, C2 (Refer to column 3, line 8 to column I4, line 34]	1 - 11
Y	JP, 4-130826, A (Hitachi Maxell, Ltd.), May 1, 1992 (01. 05. 92) (Family: none) (Refer to page 6, upper right column, line 7 to page 10, upper left column, line 3; Fig. 1)	9 - 11
A	JP, 59-90448, A (Toshiba Corp.), May 24, 1984 (24. 05. 84) (Family: none)	1 - 11

[X] Further documents are listed in the continuation of Box C.　　[ ] See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance		
"E"	earlier document but published on or after the international filing date	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed	"&"	document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
January 14, 1997 (14. 01. 97)	February 4, 1997 (04. 02. 97)

Name and mailing address of the ISA/	Authorized officer
Japanese Patent Office	
Facsimile No.	Telephone No.

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP96/03040

C (Continuation).   DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP, 63-200630, A (NEC Corp.), August 18, 1988 (18. 08. 88)(Family: none)	1 - 11

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